AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A duty cycle correction circuit of a delay locked loop, comprising:

a differential amplifier having first and second input terminals and first and second differential output terminals, and adapted to receive differential reference clock signals input via the first and second input terminals, to amplify the differential reference clock signals, and to output the amplified differential reference clock signals via the first and second differential output terminals, the differential amplifier including a switching device connected between the first and second differential output terminals, the switching device having a control terminal adapted to receive an equalization control signal and in response thereto to equalize voltages on the first and second differential output terminals;

a first transmission circuit connected between the first differential output terminal of the differential amplifier and a first node, and adapted to transmit to the first node a first one of the amplified differential reference clock signals appearing at the first differential output terminal of the differential amplifier;

a second transmission circuit connected between the second differential output terminal of the differential amplifier and a second node, and adapted to transmit to the second node a second one of the amplified differential reference clock signals appearing at the second differential output terminal of the differential amplifier;

a first storage unit connected between the first node and a ground voltage, and adapted to store a signal of the first node;

a second storage unit connected between the second node and the ground voltage and adapted to store a signal of the second node; and

a switching circuit connected between the first node and a first output terminal of the duty cycle correction circuit, and connected between the second node and a second output terminal of the duty cycle correction circuit, the switching circuit having a control terminal adapted to receive a switching control signal to selectively provide the signals of the first and second nodes to the first and second output terminals of the duty cycle correction circuit.

2. (Original) The duty cycle correction circuit of claim 1, wherein the switching circuit comprises:

a third transmission circuit adapted to transmit the signal of the first node to the first output terminal when the switching control signal has a deactivated state;

a fourth transmission circuit adapted to transmit the signal of the second node to the second output terminal when the switching control signal has the deactivated state;

a first voltage supplying circuit which is connected between the first output terminal and the ground voltage, and supplies the ground voltage to the first output terminal when a switching control signal has an activated state; and

a second voltage supplying circuit which is connected between the second output terminal and the ground voltage, and supplies the ground voltage to the second output terminal when the switching control signal has the activated state.

3. (Original) The duty cycle correction circuit of claim 2, wherein the first through fourth transmission circuits each include a PMOS transistor and a NMOS transistor.

4. (Original) The duty cycle correction circuit of claim 1, wherein the first and second storage units each include a MOS transistor.

5-12. (Canceled)

13. (Currently Amended) A duty cycle correction circuit, comprising:

a pair of input terminals adapted to receive a pair of differential reference clock signals each having a duty cycle;

a differential amplifier adapted to amplify the differential reference clock signals and provide the differential reference clock signals to the integrating means, the differential amplifier including a switching device connected between first and second differential output terminals thereof, the switching device having a control terminal adapted to receive an equalization control signal and in response thereto to equalize voltages on the first and second differential output terminals;

integrating means for integrating each of the reference clock signals to produce a pair of control signals indicating the duty cycles of the differential reference clock signals; and

switching means adapted to receive a switching control signal and in response thereto to selectively output the control signals when the switching control signal has a first state and to output a pair of fixed voltage signals when the switching control signal has a second state.

14. (Canceled)

15. (Original) The duty cycle correction circuit of claim 13, where the integrating means includes at least a pair of capacitors each for integrating a corresponding one of the reference clock signals.

16. (Original) The duty cycle correction circuit of claim 13, where the fixed voltage signals are ground voltages, and wherein the switching means includes a pair of transistors connected between corresponding output terminal and ground.